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EXAMINER	
ABELSON, RONALD B	
ART UNIT	**PAPER NUMBER**
2666	

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Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/035,538	ESSEN, SOPHIE H.	
	Examiner	Art Unit	
	Ronald Abelson	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/16/02, 3/27/02, and 10/23/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/16/02, 3/27/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gamble (US 5,592,629) in view of applicant's admitted prior art 'AAPA'.

Regarding claim 5, Gamble teaches a synchronous storage device (fig. 4 box 102C) to store data received at a first data transfer rate (fig. 4 box 111, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32: note the first data transfer rate is the rate of the DMA fig. 4 box 111).

Gamble teaches an asynchronous storage device coupled to the synchronous storage device (fig. 4 box 102A).

Gamble teaches control circuitry coupled to the synchronous storage device and to the asynchronous storage device (fig. 4 box 102B) and the output from the asynchronous storage device is

at a second data transfer rate (circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32: note the second data transfer rate is the rate of the SCSI Controller fig. 4 box 103).

Although Gamble teaches the matching the data rates between two interfaces (fig. 4 box 111, 103), the reference does not explicitly state that the control circuitry transmits the data at the first data transfer rate from the synchronous storage device to the asynchronous storage device.

AAPA teaches an asynchronous FIFO allows for the storage and extraction of data while converting the data from a first clock domain to a second clock domain and a synchronous FIFO is used for storing and transmitting data within the same clock domain ([0002]).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of Gamble by replacing the asynchronous FIFO (fig. 4 box 102A) with the asynchronous FIFO of AAPA and replacing the synchronous FIFO (fig. 4 box 102C) with the synchronous FIFO of AAPA. This modification would benefit the system by allowing a single asynchronous FIFO to perform the data rate conversion.

Regarding claim 6, the synchronous storage device is a synchronous FIFO register array (AAPA: synchronous FIFO, [0002]).

Regarding claim 7, the asynchronous storage device is an asynchronous FIFO register array (AAPA: asynchronous FIFO, [0002]).

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Gamble (US 5,592,629) and AAPA as applied to claim 5 above, and further in view of Subrahmanyan (US 2002/0186719).

The combination is silent on the first data transfer rate is greater than the second data transfer rate.

Subrahmanyan teaches a system wherein the first data transfer rate / Sonet is greater than the second data transfer rate / DS-3 (DS-3 data must be converted from the Sonet clock signal to the lower frequency DS-3 clock signal, [0009]).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble and AAPA by replacing the DMA interface (Gamble: fig. 4 box 111) with a Sonet interface that transmits embedded DS-3

data and replacing the SCSI controller (Gamble: fig. 4 box 103) with a DS-3 interface. This modification can be performed by modifying the control circuit of Gamble (fig. 4 box 102B, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32) so that the Asynchronous FIFO will receive data from the Synchronous FIFO at the Sonet rate and the data received from the Synchronous FIFO will be transmitted at the DS-3 rate. This modification will benefit the system by enabling it to work in a Sonet/DS-3 environment.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gamble (US 5,592,629) and AAPA as applied to claim 5 above, and further in view of Wills (US 6,052,376).

Although the combination discusses the desire to have a small asynchronous FIFO (AAPA: if an asynchronous FIFO is of size 2^{12} bits, the pointers and logic tables can be 12 bits each. This amounts to a large amount of space required for the control circuitry. Also, the amount of time required to implement a large asynchronous FIFO is increased due to the large double-sync logic and gray code tables, [0003]), the combination is silent on the implementation of a small asynchronous FIFO. Note, the examiner maintains that a "small asynchronous FIFO" would have a storage area smaller than the synchronous FIFO since

"small" is a relative term and the only two storage units in the system of the combination of Gamble and AAPA are the asynchronous FIFO and synchronous FIFO.

Wills teaches a method that can be used for implementing a transmitting buffer and a smaller receiving buffer. Specifically, Wills teaches a receiving buffer (fig. 1 box 22: 2 k cells) sending a backpressure signal to a transmitting buffer (fig. 1 box 21 7 k cells) informing the transmitting buffer to stop transmitting and thus prevent overflow in the receiving buffer (col. 2 lines 51-57).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble and AAPA by making the synchronous buffer larger than the asynchronous buffer. Having the asynchronous buffer send backpressure signals to the synchronous buffer to prevent overflow of the asynchronous buffer can perform this modification. As previously stated one suggestion for the modification is having a small asynchronous buffer would not require a large amount of time to implement since a large asynchronous FIFO requires large double-sync logic and gray code tables (AAPA: [0003]).

5. Claims 1-3, 10, 13, 14, 28-30, 32, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gamble (US 5,592,629) in view of applicant's admitted prior art 'AAPA', and further in view of Wills (US 6,052,376).

Regarding claims 1, 10, 28, and 32, Gamble teaches storing data of a first data transfer rate in a synchronous storage device having a first storage area (fig. 4 box 102C see data transfer from box 111 to 102C, fig. 4 box 111, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32: note the first data transfer rate is the rate of the DMA fig. 4 box 111).

Gamble teaches storing the data in the asynchronous storage device having a second storage area (fig. 4 box 102A).

Gamble teaches outputting the data from the asynchronous storage device at a second data transfer rate (circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32: note the second data transfer rate is the rate of the SCSI Controller fig. 4 box 103).

Regarding claims 10 and 32 in addition to the limitations previously listed Gamble teaches receiving data at a first data transfer rate (fig. 4 box 102C see data transfer from box 111 to 102C, fig. 4 box 111, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32: note the

first data transfer rate is the rate of the DMA fig. 4 box 111); and removing the data from the synchronous storage device (fig. 4 box 102C, 102A: see transfer of data from box 102C to 102A).

Although Gamble teaches the matching the data rates between two interfaces (fig. 4 box 111, 103), the reference does not explicitly state the first data transfer rate is the data rate of the data transmitted from the synchronous storage device to the asynchronous storage device.

AAPA teaches an asynchronous FIFO allows for the storage and extraction of data while converting the data from a first clock domain to a second clock domain and a synchronous FIFO is used for storing and transmitting data within the same clock domain ([0002]).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of Gamble by replacing the asynchronous FIFO (fig. 4 box 102A) with the asynchronous FIFO of AAPA and replacing the synchronous FIFO (fig. 4 box 102C) with the synchronous FIFO of AAPA. This modification would benefit the system by allowing a single asynchronous FIFO to perform the data rate conversion.

Although the combination discusses the desire to have a small asynchronous FIFO (AAPA: if an asynchronous FIFO is of size 2^{12} bits, the pointers and logic tables can be 12 bits each. This amounts to a large amount of space required for the control circuitry. Also, the amount of time required to implement a large asynchronous FIFO is increased due to the large double-sync logic and gray code tables, [0003]), the combination is silent on the implementation of a small asynchronous FIFO. Note, the examiner maintains that a "small asynchronous FIFO" would have a storage area smaller than the synchronous FIFO since "small" is a relative term and the only two storage units in the system of the combination of Gamble and AAPA are the asynchronous FIFO and synchronous FIFO.

Wills teaches a method that can be used for implementing a transmitting buffer and a smaller receiving buffer. Specifically, Wills teaches a receiving buffer (fig. 1 box 22: 2 k cells) sending a backpressure signal to a transmitting buffer (fig. 1 box 21 7 k cells) informing the transmitting buffer to stop transmitting and thus prevent overflow in the receiving buffer (col. 2 lines 51-57).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble and AAPA by making the synchronous buffer larger than the

asynchronous buffer. Having the asynchronous buffer send backpressure signals to the synchronous buffer to prevent overflow of the asynchronous buffer can perform this modification. As previously stated one suggestion for the modification is having a small asynchronous buffer would not require a large amount of time to implement since a large asynchronous FIFO requires large double-sync logic and gray code tables (AAPA: [0003]).

Regarding claims 2, 13, 29, 35, the synchronous storage device is a synchronous FIFO (AAPA: synchronous FIFO, [0002]).

Regarding claims 3, 14, 30, 36, the asynchronous storage device is an asynchronous FIFO (AAPA: asynchronous FIFO, [0002]).

6. Claims 4, 11, 12, 15, 31, 33, 34, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Gamble, AAPA, and Wills as applied to claims 1, 10, 10, 10, 28, 32, 32, and 32 respectively above, and further in view of Subrahmanyan (US 2002/0186719).

Regarding claims 4, 15, 31, and 37, the combination is silent on the first data transfer rate / Sonet is greater than the second data transfer rate / DS-3.

Subrahmanyan teaches a system wherein the first data transfer rate is greater than the second data transfer rate (DS-3 data must be converted from the Sonet clock signal to the lower frequency DS-3 clock signal, [0009]).

Regarding claims 11 and 33, the combination is silent on the data of first transfer rate is included in a signal using the Sonet standard.

Subrahmanyan teaches the data of first transfer rate is included in a signal using the Sonet standard (Sonet, [0009])

Regarding claims 12 and 34, the combination is silent on the data of second transfer rate is included in a signal using the DS-3 standard.

Subrahmanyan teaches the data of second transfer rate is included in a signal using the DS-3 standard (DS-3, [0009])

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble, AAPA, and Wills by replacing the DMA interface (Gamble:

fig. 4 box 111) with a Sonet interface that transmits embedded DS-3 data and replacing the SCSI controller (Gamble: fig. 4 box 103) with a DS-3 interface. This modification can be performed by modifying the control circuit of Gamble (fig. 4 box 102B, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32) so that the Asynchronous FIFO will receive data from the Synchronous FIFO at the Sonet rate and the data received from the Synchronous FIFO will be transmitted at the DS-3 rate. This modification will benefit the system by enabling it to work in a Sonet/DS-3 environment.

7. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gamble (US 5,592,629) in view of Wills (US 6,052,376), Subrahmanyan (US 2002/0186719), and further in view of Newton.

Regarding claim 25, Gamble teaches a synchronous FIFO having a first storage area (fig. 4 box 102C) and coupled to receive data at a first data transfer rate (fig. 4 box 111, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32: note the first data transfer rate is the rate of the DMA fig. 4 box 111).

Gamble teaches an asynchronous FIFO having a second storage area and coupled to the synchronous storage device (fig. 4 box 102A).

Gamble teaches control circuitry coupled to the synchronous FIFO and to the asynchronous FIFO wherein the control circuitry is to transfer the data from the synchronous FIFO to the asynchronous FIFO (fig. 4 box 102B) and the output from the asynchronous storage device is at a second data transfer rate (circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32: note the second data transfer rate is the rate of the SCSI Controller fig. 4 box 103).

Although the desire to have a small asynchronous FIFO is well known in the art (AAPA: if an asynchronous FIFO is of size 2^{12} bits, the pointers and logic tables can be 12 bits each. This amounts to a large amount of space required for the control circuitry. Also, the amount of time required to implement a large asynchronous FIFO is increased due to the large double-sync logic and gray code tables, [0003]), Gamble is silent on the implementation of a small asynchronous FIFO. Note, the examiner maintains that a "small asynchronous FIFO" would have a storage area smaller than the synchronous FIFO since "small" is

a relative term and the only two storage units in the system of Gamble are the asynchronous FIFO and synchronous FIFO.

Wills teaches a method that can be used for implementing a transmitting buffer and a smaller receiving buffer. Specifically, Wills teaches a receiving buffer (fig. 1 box 22: 2 k cells) sending a backpressure signal to a transmitting buffer (fig. 1 box 21 7 k cells) informing the transmitting buffer to stop transmitting and thus prevent overflow in the receiving buffer (col. 2 lines 51-57).

Gamble is silent on only permitting transfer of data between the two buffers when the receiving buffer is not full.

Wills teaches permitting transfer of data between the two buffers when the receiving buffer is not full (congested, backpressure signal, col. 2 lines 51-57).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of Gamble by making the synchronous buffer larger than the asynchronous buffer. Having the asynchronous buffer send backpressure signals to the synchronous buffer to prevent overflow of the asynchronous buffer can perform this modification. As previously stated one suggestion for the modification is having a small asynchronous

buffer would not require a large amount of time to implement since a large asynchronous FIFO requires large double-sync logic and gray code tables (AAPA: [0003]).

The combination of Gamble and Wills is silent on the received data is based on a DS-3 standard from a payload of Sonet frames.

Subrahmanyan teaches received data is based on a DS-3 standard from a payload of Sonet frames (figs. 3, 4, line 306, DS-3 embedded within Sonet, [0010]).

The combination of Gamble and Wills is silent on outputting the data at the DS-3 rate.

Subrahmanyan teaches outputting the data at the DS-3 rate (DS-3 data must be converted from the Sonet clock signal to the lower frequency DS-3 clock signal, [0009]).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble and Wills by replacing the DMA interface (Gamble: fig. 4 box 111) with a Sonet interface that transmits embedded DS-3 data and replacing the SCSI controller (Gamble: fig. 4 box 103) with a DS-3 interface. This modification can be performed by

modifying the control circuit of Gamble (fig. 4 box 102B, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32) so that the Asynchronous FIFO will receive data from the Synchronous FIFO at the Sonet rate and the data received from the Synchronous FIFO will be transmitted at the DS-3 rate. This modification will benefit the system by enabling it to work in a Sonet/DS-3 environment.

Although the combination of Gamble, Wills, and Subrahmanyan teaches Sonet and STS (Subrahmanyan: Sonet, STS-N,[0001]), the combination is silent on an Optical Carrier signal.

Newton teaches an Optical Carrier signal (pg. 535, OC-N, N=3, 48). Note, N may be 3 or 48.

Although the combination of Gamble, Wills, and Subrahmanyan teaches DS-3 (Subrahmanyan: DS-3, [0001]), the combination is silent on T3.

Newton teaches T3 (pg. 732, T-3).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble, Wills, and Subrahmanyan by transmitting the Sonet frames on a (OC-N, N=3, 48) signal and outputting the DS-3 data rate on

a T3 signal. Adhering to the OC and T3 standards can perform this modification. The suggestions for these modifications are OC-N is the optical interface designed to work with STS in Sonet (Newton: pg. 535) and T3 is the North American standard for DS-3.

Regarding claim 26, as previously shown, the OC signal includes an OC-48 signal (Newton: OC-N, N=48).

Regarding claim 27, as previously shown, the OC signal includes an OC-3 signal (Newton: OC-N, N=3).

8. Claims 16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gamble (US 5,592,629) in view of AAPA, and further in view of Wills (US 6,052,376).

Regarding claim 16, Gamble teaches a synchronous storage device having a first storage area (fig. 4 box 102C) and coupled to receive data at a first data transfer rate (fig. 4 box 111, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32: note the first data transfer rate is the rate of the DMA fig. 4 box 111).

Gamble teaches an asynchronous storage device having a second storage area and coupled to the synchronous storage device (fig. 4 box 102A).

Gamble teaches control circuitry coupled to the synchronous storage device and to the asynchronous storage device (fig. 4 box 102B) and the output from the asynchronous storage device is at a second data transfer rate (circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32: note the second data transfer rate is the rate of the SCSI Controller fig. 4 box 103).

Although Gamble teaches the matching the data rates between two interfaces (fig. 4 box 111, 103), the reference does not explicitly state that the control circuitry transfers the data at the first data transfer rate from the synchronous storage device to the asynchronous storage device.

AAPA teaches an asynchronous FIFO allows for the storage and extraction of data while converting the data from a first clock domain to a second clock domain and a synchronous FIFO is used for storing and transmitting data within the same clock domain ([0002]).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of Gamble by replacing

the asynchronous FIFO (fig. 4 box 102A) with the asynchronous FIFO of AAPA and replacing the synchronous FIFO (fig. 4 box 102C) with the synchronous FIFO of AAPA. This modification would benefit the system by allowing a single asynchronous FIFO to perform the data rate conversion.

Although the combination discusses the desire to have a small asynchronous FIFO (AAPA: if an asynchronous FIFO is of size 2^{12} bits, the pointers and logic tables can be 12 bits each. This amounts to a large amount of space required for the control circuitry. Also, the amount of time required to implement a large asynchronous FIFO is increased due to the large double-sync logic and gray code tables, [0003]), the combination is silent on the implementation of the first storage device area / synchronous FIFO is larger than the second storage area / asynchronous FIFO. Note, the examiner maintains that a "small asynchronous FIFO" would have a storage area smaller than the synchronous FIFO since "small" is a relative term and the only two storage units in the system of the combination of Gamble and AAPA are the asynchronous FIFO and synchronous FIFO.

Wills teaches a method that can be used for implementing a transmitting buffer and a smaller receiving buffer. Specifically, Wills teaches a receiving buffer (fig. 1 box 22: 2

k cells) sending a backpressure signal to a transmitting buffer (fig. 1 box 21 7 k cells) informing the transmitting buffer to stop transmitting and thus prevent overflow in the receiving buffer (col. 2 lines 51-57).

The combination is silent on only permitting transfer of data between the two buffers when the receiving buffer is not full.

Wills teaches permitting transfer of data between the two buffers when the receiving buffer is not full (congested, backpressure signal, col. 2 lines 51-57).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble and AAPA by making the synchronous buffer larger than the asynchronous buffer. Having the asynchronous buffer send backpressure signals to the synchronous buffer to prevent overflow of the asynchronous buffer can perform this modification. As previously stated one suggestion for the modification is having a small asynchronous buffer would not require a large amount of time to implement since a large asynchronous FIFO requires large double-sync logic and gray code tables (AAPA: [0003]).

Regarding claim 19, the synchronous storage device is a synchronous FIFO (AAPA: synchronous FIFO, [0002]).

Regarding claim 20, the asynchronous storage device is an asynchronous FIFO (AAPA: asynchronous FIFO, [0002]).

9. Claims 17, 18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Gamble (US 5,592,629), AAPA, and Wills (US 6,052,376) as applied to claim 16 above, and further in view of Subrahmanyan (US 2002/0186719).

Regarding claim 17, the combination is silent on the data of first transfer rate is included in a signal using the Sonet standard.

Subrahmanyan teaches the data of first transfer rate is included in a signal using the Sonet standard (Sonet, [0009])

Regarding claim 18, the combination is silent on the data of second transfer rate is included in a signal using the DS-3 standard.

Subrahmanyan teaches the data of second transfer rate is included in a signal using the DS-3 standard (DS-3, [0009])

Regarding claims 21, the combination is silent on the first data transfer rate is greater than the second data transfer rate.

Subrahmanyan teaches a system wherein the first data transfer rate / Sonet is greater than the second data transfer rate / DS-3 (DS-3 data must be converted from the Sonet clock signal to the lower frequency DS-3 clock signal, [0009]).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble, AAPA, and Wills by replacing the DMA interface (Gamble: fig. 4 box 111) with a Sonet interface that transmits embedded DS-3 data and replacing the SCSI controller (Gamble: fig. 4 box 103) with a DS-3 interface. This modification can be performed by modifying the control circuit of Gamble (fig. 4 box 102B, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32) so that the Asynchronous FIFO

will receive data from the Synchronous FIFO at the Sonet rate and the data received from the Synchronous FIFO will be transmitted at the DS-3 rate. This modification will benefit the system by enabling it to work in a Sonet/DS-3 environment.

10. Claims 22-24 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gamble (US 5,592,629) in view of Subrahmanyan (US 2002/0186719), Wills (US 6,052,376), and further in view of Newton.

Regarding claims 22 and 38, Gamble teaches receiving data (fig. 4 box 102C see data transfer from box 111 to 102C).

Gamble teaches storing data in a synchronous FIFO having a first storage area (fig. 4 box 102C).

Gamble teaches transferring the data from the synchronous FIFO to an asynchronous FIFO having a second storage area (fig. 4 see transfer of data from box 102C to 102A).

Gamble teaches outputting the data based from the asynchronous FIFO at a data rate consistent with the receiving device (fig. 4 box 102A, 102B, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32).

Gamble is silent on the received data is based on a DS-3 standard from a payload of Sonet frames.

Subrahmanyan teaches (figs. 3, 4, line 306, DS-3 embedded within Sonet, [0010]).

Gamble is silent on extracting the data based on the DS-3 standard from the payload of the Sonet frames.

Subrahmanyan teaches extracting the data based on the DS-3 standard from the payload of the Sonet frames (DS-3 data must be converted from the Sonet clock signal to the lower frequency DS-3 clock signal, [0009]). Note in order for the data to be converted, it first must be extracted.

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of Gamble by replacing the DMA interface (Gamble fig. 4 box 111) with a Sonet interface that transmits embedded DS-3 data and replacing the SCSI controller Interface (fig. 4 box 103) with a DS-3 interface. This modification can be performed by modifying the control circuit of Gamble (fig. 4 box 102B, circuit for matching data rates between two devices that are asynchronous, col. 2 lines 29-32) so that the Asynchronous FIFO will receive data from the Synchronous FIFO at the Sonet rate and the data received from

the Synchronous FIFO will be transmitted at the DS-3 rate. This modification will benefit the system by enabling it to work in a Sonet/DS-3 environment.

Although the desire to have a small asynchronous FIFO is well known in the art (AAPA: if an asynchronous FIFO is of size 2^{12} bits, the pointers and logic tables can be 12 bits each. This amounts to a large amount of space required for the control circuitry. Also, the amount of time required to implement a large asynchronous FIFO is increased due to the large double-sync logic and gray code tables, [0003]), the combination is silent on the implementation of a small asynchronous FIFO. Note, the examiner maintains that a "small asynchronous FIFO" would have a storage area smaller than the synchronous FIFO since "small" is a relative term and the only two storage units in the system of the combination of Gamble and Subrahmanyan are the asynchronous FIFO and synchronous FIFO.

Wills teaches a method that can be used for implementing a transmitting buffer and a smaller receiving buffer. Specifically, Wills teaches a receiving buffer (fig. 1 box 22: 2 k cells) sending a backpressure signal to a transmitting buffer (fig. 1 box 21 7 k cells) informing the transmitting buffer to

stop transmitting and thus prevent overflow in the receiving buffer (col. 2 lines 51-57).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble and Subrahmanyan by making the synchronous buffer larger than the asynchronous buffer. Having the asynchronous buffer send backpressure signals to the synchronous buffer to prevent overflow of the asynchronous buffer can perform this modification. As previously stated one suggestion for the modification is having a small asynchronous buffer would not require a large amount of time to implement since a large asynchronous FIFO requires large double-sync logic and gray code tables (AAPA: [0003]).

Although the combination of Gamble, Subrahmanyan, and Wills, teaches Sonet and STS (Subrahmanyan: Sonet, STS-N, [0001]), the combination is silent on an Optical Carrier signal.

Newton teaches an Optical Carrier signal (pg. 535, OC-N, N=3, 48). Note, N may be 3 or 48.

Although the combination of Gamble, Subrahmanyan, and Wills teaches DS-3 (Subrahmanyan: DS-3, [0001]), the combination is silent on T3.

Newton teaches T3 (pg. 732, T-3).

Therefore it would have been obvious to one of ordinary skill in the art, to modify the system of the combination of Gamble, Subrahmanyan, and Wills by transmitting the Sonet frames on a (OC-N, N=3, 48) signal and outputting the DS-3 data rate on a T3 signal. Adhering to the OC and T3 standards can perform this modification. The suggestions for these modifications are OC-N is the optical interface designed to work with STS in Sonet (Newton: pg. 535) and T3 is the North American standard for DS-3.

Regarding claims 23 and 39, as previously shown, the OC signal includes an OC-48 signal (Newton: OC-N, N=48).

Regarding claims 24 and 40, as previously shown, the OC signal includes an OC-3 signal (Newton: OC-N, N=3).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald

Abelson's whose telephone number is (571) 272-3165. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seem Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Ronald Abelson
Examiner
Art Unit 2666

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